

## Freeform Search

<b>Database:</b>	US Pre-Grant Publication Full-Text Database		
	<b>US Patents Full-Text Database</b>		
	US OCR Full-Text Database		
	EPO Abstracts Database		
	JPO Abstracts Database		
	Derwent World Patents Index		
	IBM Technical Disclosure Bulletins		
<b>Term:</b>	L8 and @py<=2001		
<b>Display:</b>	20	<b>Documents in Display Format:</b> TI	<b>Starting with Number</b> 1
<b>Generate:</b> <input type="radio"/> Hit List <input checked="" type="radio"/> Hit Count <input type="radio"/> Side by Side <input type="radio"/> Image			

### Search History

DATE: Tuesday, December 27, 2005   [Printable Copy](#)   [Create Case](#)

#### Set Name Query

side by side

#### Hit Count Set Name

result set

DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ

<u>L9</u>	L8 and @py<=2001	9	<u>L9</u>
<u>L8</u>	L1 and memory adj circuit\$1 same invert\$3 same pixel\$1	50	<u>L8</u>
<u>L7</u>	L1 and memory adj circuit\$1 same invert\$3	2760	<u>L7</u>
<u>L6</u>	L1 memory adj circuit\$1 same invert\$3	0	<u>L6</u>
<u>L5</u>	L4 and @py<=2001	5	<u>L5</u>
<u>L4</u>	memory adj circuit\$1 same pixel\$1 same inverter\$1	42	<u>L4</u>
<u>L3</u>	memory adj circuit\$1 same pixel\$1 same invert\$3	50	<u>L3</u>
<u>L2</u>	memory adj circuit\$1 same pixel\$1	1252	<u>L2</u>
<u>L1</u>	memory adj circuit\$1	55214	<u>L1</u>

END OF SEARCH HISTORY

## Search Forms

Search  
Results

## Freeform Search

## User Searches

## Preferences

## Logout

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
 JPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Term:

L11 and @py&lt;=2001

Display:  Documents in Display Format:  Starting with Number Generate: ☐ Hit List ☒ Hit Count ☐ Side by Side ☐ Image

Search

Clear

Interrupt

## Search History

DATE: Tuesday, December 27, 2005 [Printable Copy](#) [Create Case](#)Set Name Query

side by side

Hit Count Set Name

result set

DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ

<u>L13</u>	L11 and @py<=2001	19	<u>L13</u>
<u>L12</u>	L11 and @py<=2000	17	<u>L12</u>
<u>L11</u>	L10 and invert\$3	71	<u>L11</u>
<u>L10</u>	pixel near2 memory adj circuit	214	<u>L10</u>
<u>L9</u>	pixel near4 memory adj circuit	309	<u>L9</u>
<u>L8</u>	L7 and inverter\$1	25	<u>L8</u>
<u>L7</u>	pixel adj memory adj circuit	112	<u>L7</u>
<u>L6</u>	pixel adj memory adj circuit	0	<u>L6</u>
<u>L5</u>	L4 and @py<=2001	5	<u>L5</u>
<u>L4</u>	pixel same memory adj circuit same inverter\$1	42	<u>L4</u>
<u>L3</u>	pixel same memory adj circuit	1252	<u>L3</u>
<u>L2</u>	L1 and @py<=2001	1	<u>L2</u>
<u>L1</u>	pixel\$1 same memory adj circuit same inverter adj circuit	15	<u>L1</u>

END OF SEARCH HISTORY